(12) UK Patent Application (19) GB (11) 2 255 668 (13) A

(43) Date of A publication 11.11.1992

(21) Application No 9206597.8

(22) Date of filing 25.03.1992

(30) Priority data
(31) 03091011 (32) 30.03.1991 (33) JP

(51) INT CL[5]
G09G 3/36

(52) UK CL (Edition K)
G5C CA342 CHB

(56) Documents cited
GB 2106689 A EP 0216188 A2 EP 0055676 A2

(58) Field of search
UK CL (Edition K) G5C CHB
INT CL[5] G09G
Online databases: WPI

(71) Applicants
Kabushiki Kaisha Toshiba

(Incorporated in Japan)

72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken, Japan

Toshiba Micro-Electronics Corporation

(Incorporated in Japan)

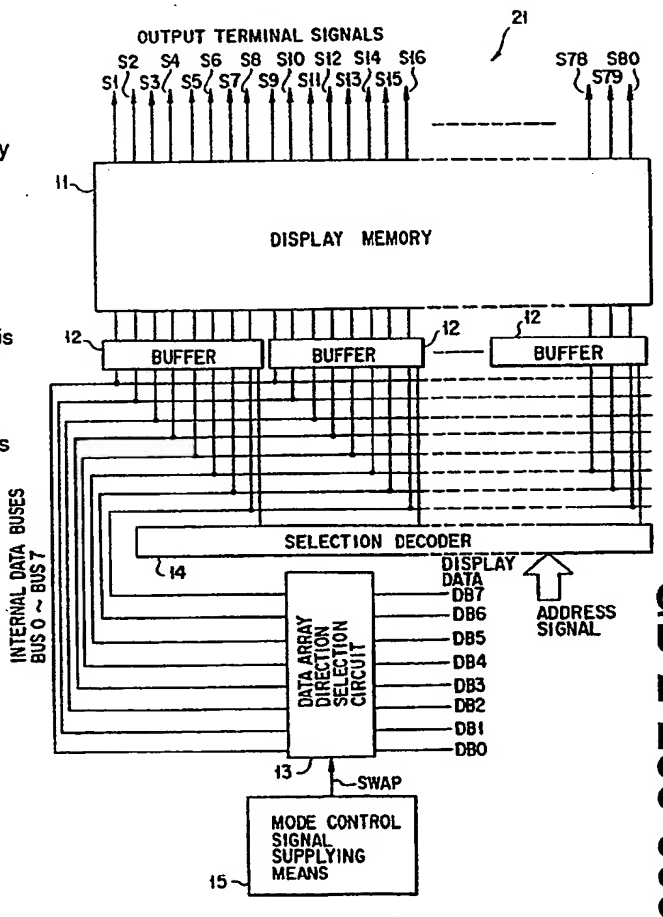
25-1, Ekimaehoncho, Kawasaki-ku, Kawasaki-shi, Japan

(72) Inventors
Takashi Arakawa
Kinya Sakaki

(74) Agent and/or Address for Service
Marks & Clerk
57-60 Lincoln's Inn Fields, London, WC2A 3LS, United Kingdom

(54) Display driving/controlling integrated circuit and display system

(57) A display driving/controlling integrated circuit includes a display memory (11) for storing data to be supplied to a display unit, a bus line (BUS0 to BUS7) of n-bit configuration for transmitting display data (DB0 to DB7) to be stored in the display memory with n bits set as one unit, and a data array direction selection circuit (13) connected to the bus line, for outputting display data on the bus line to the display memory either with the bit array kept in the original bit array status or inverted with respect to the original bit array. A display panel is divided into upper and lower sections each section being driven by at least one such circuit, the circuit associated with one section outputting the original bit array while the circuit associated with the other section outputs its inversion. Wirings between the LSI output terminals and the display panel can thus be simplified and the wiring connections can be easily made.



F I G. 4

GB 2 255 668 A

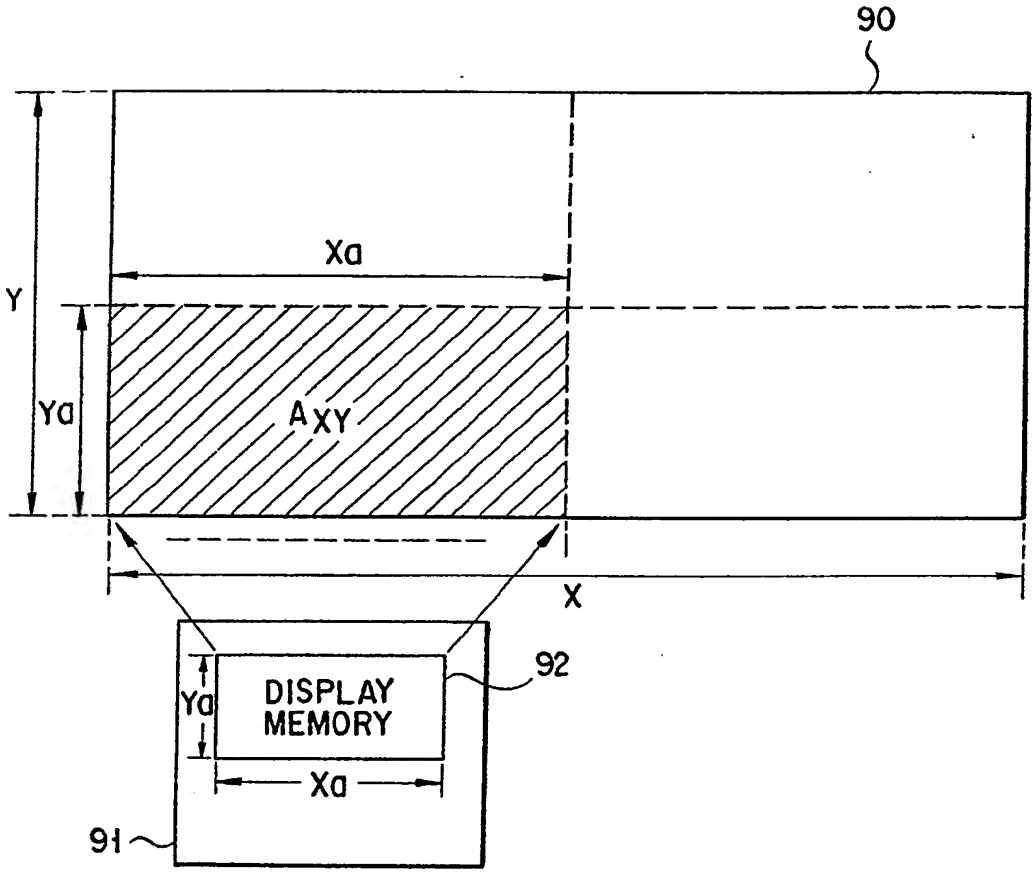


FIG. 1

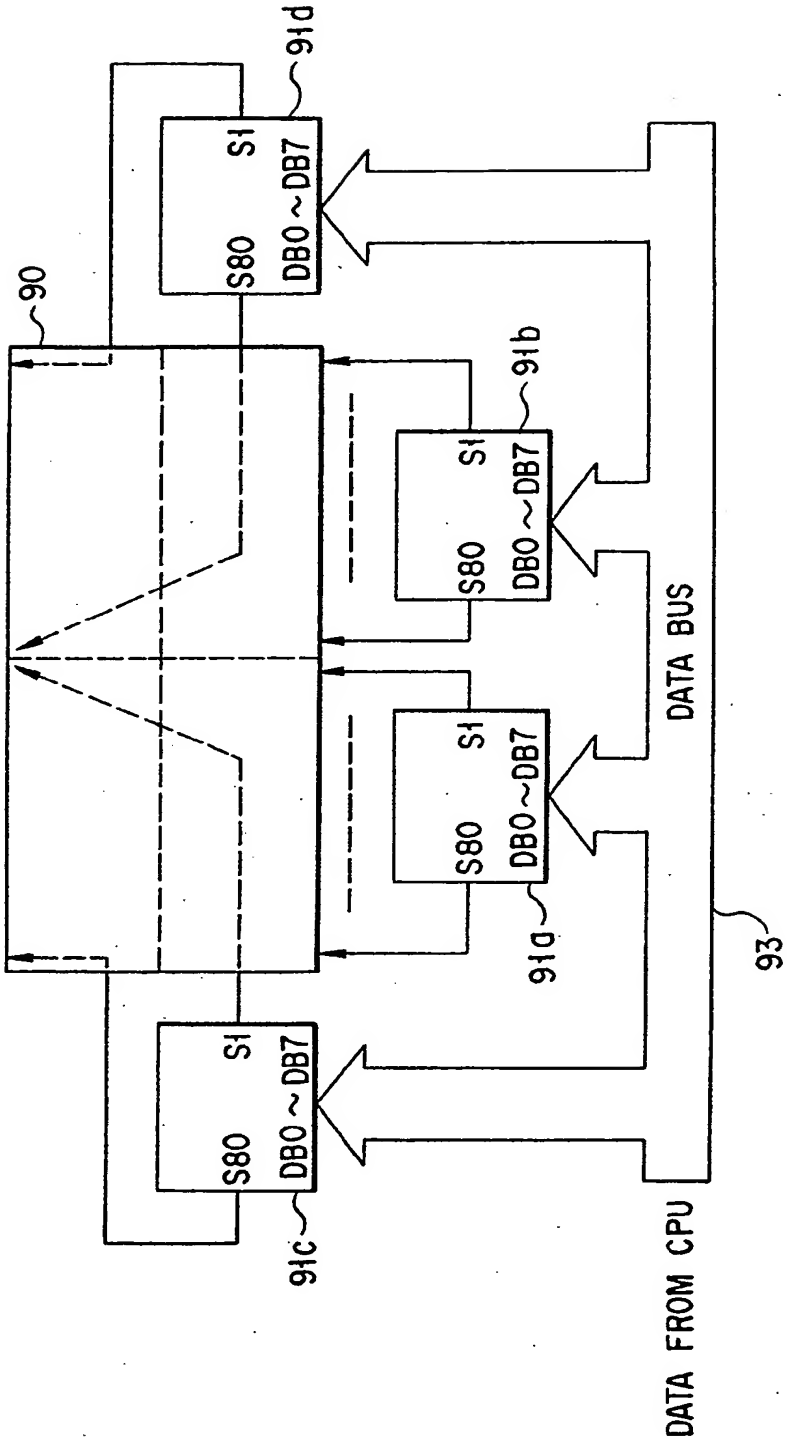


FIG. 2

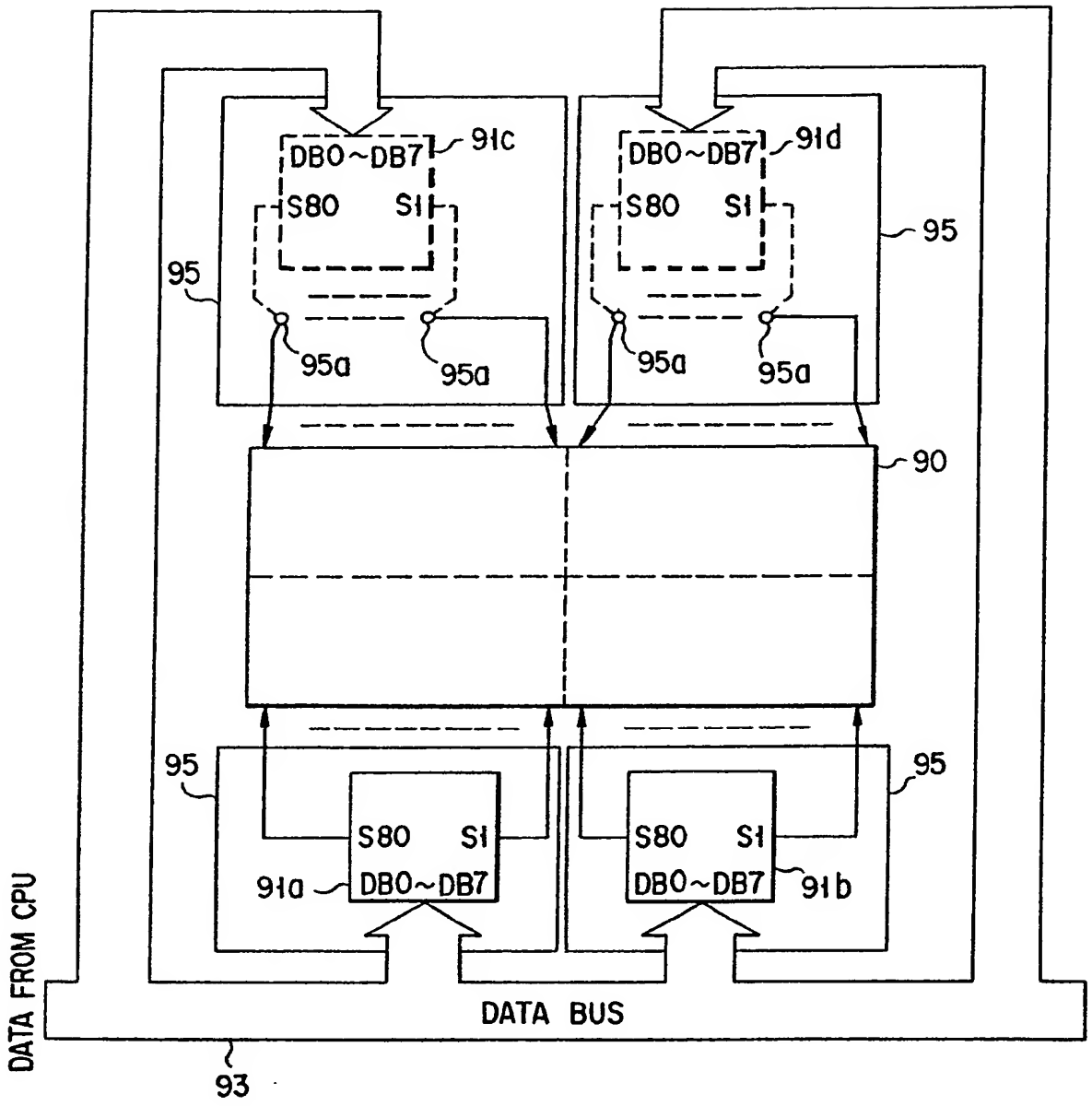


FIG. 3

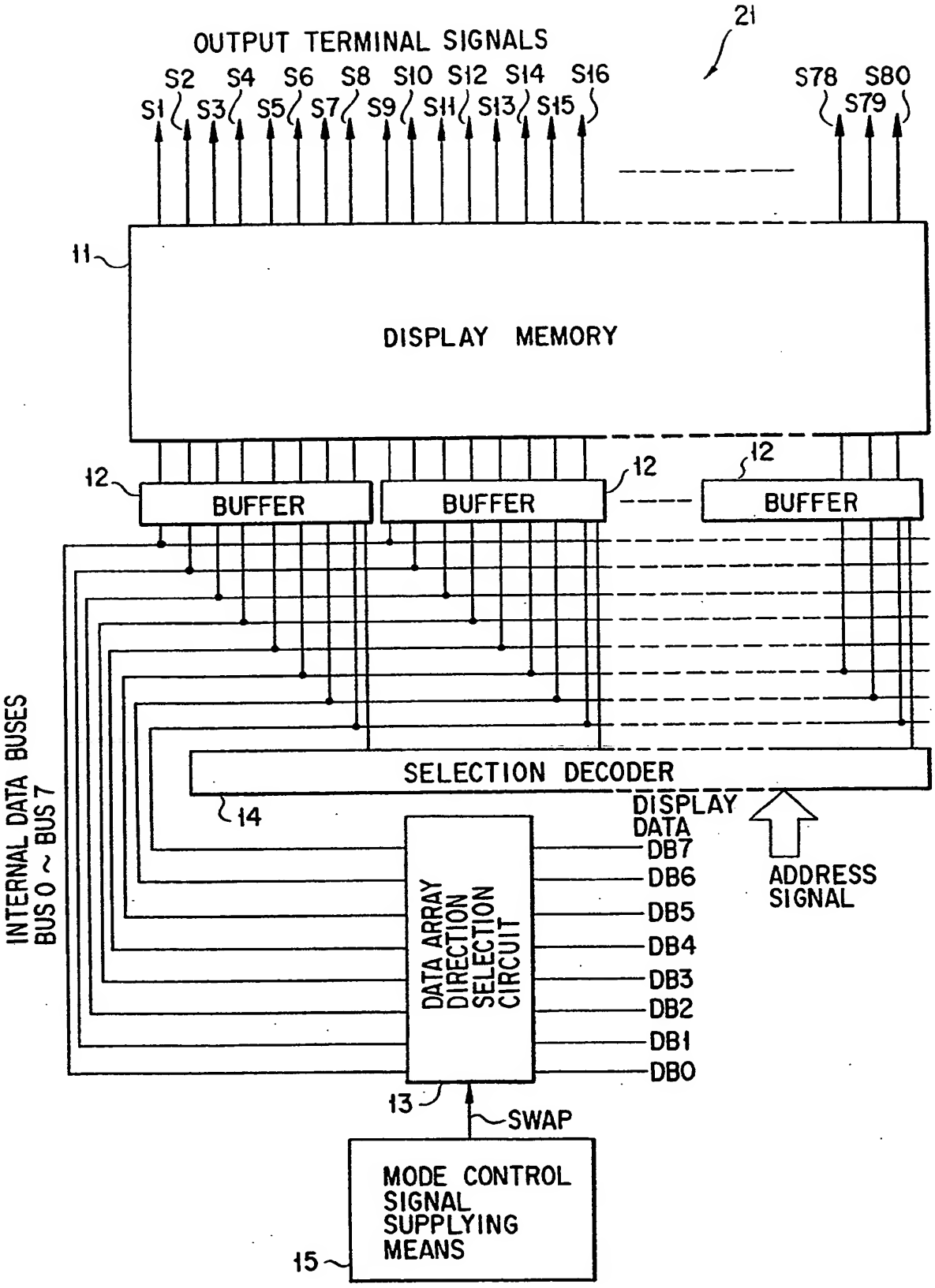


FIG. 4

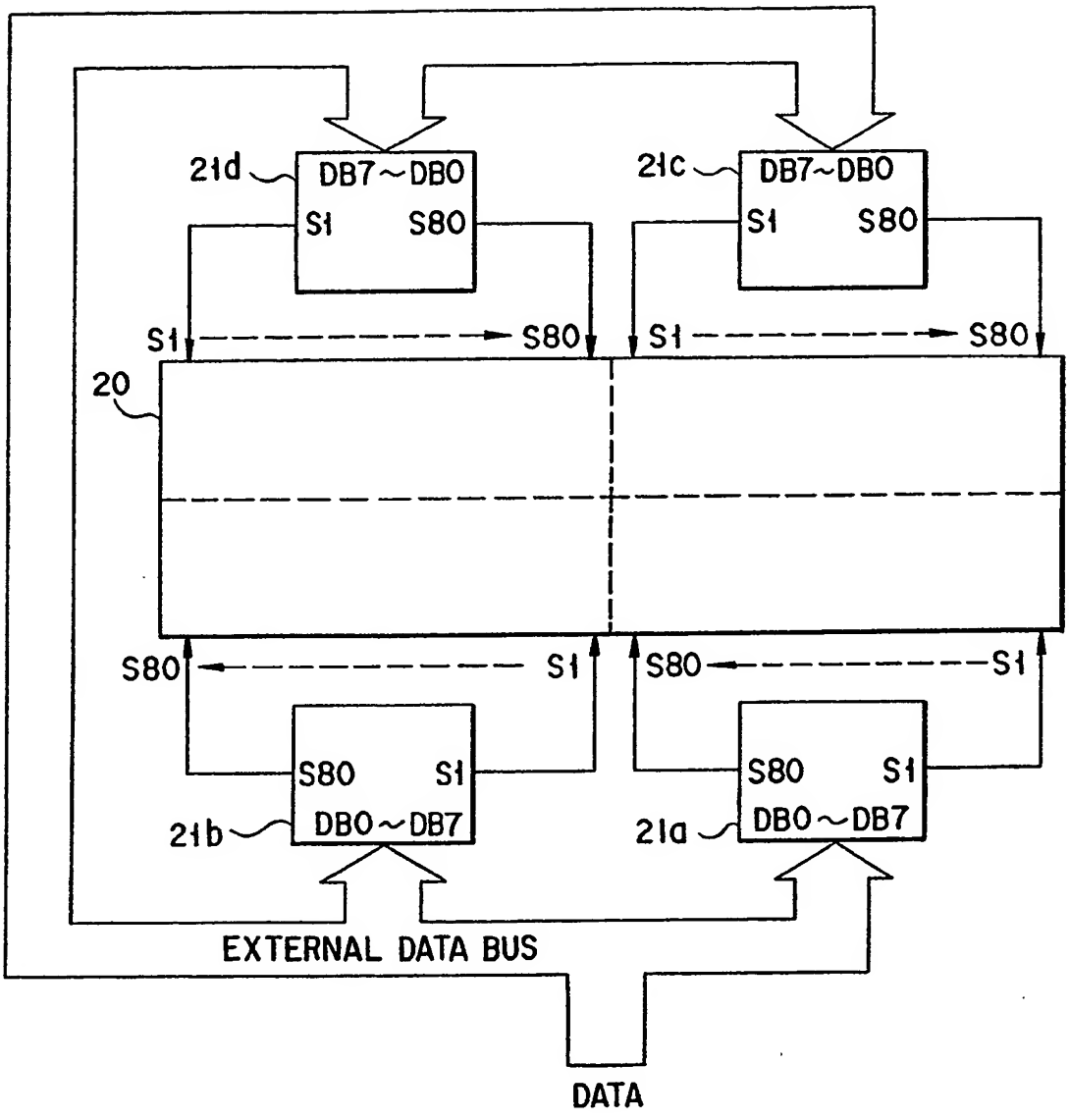
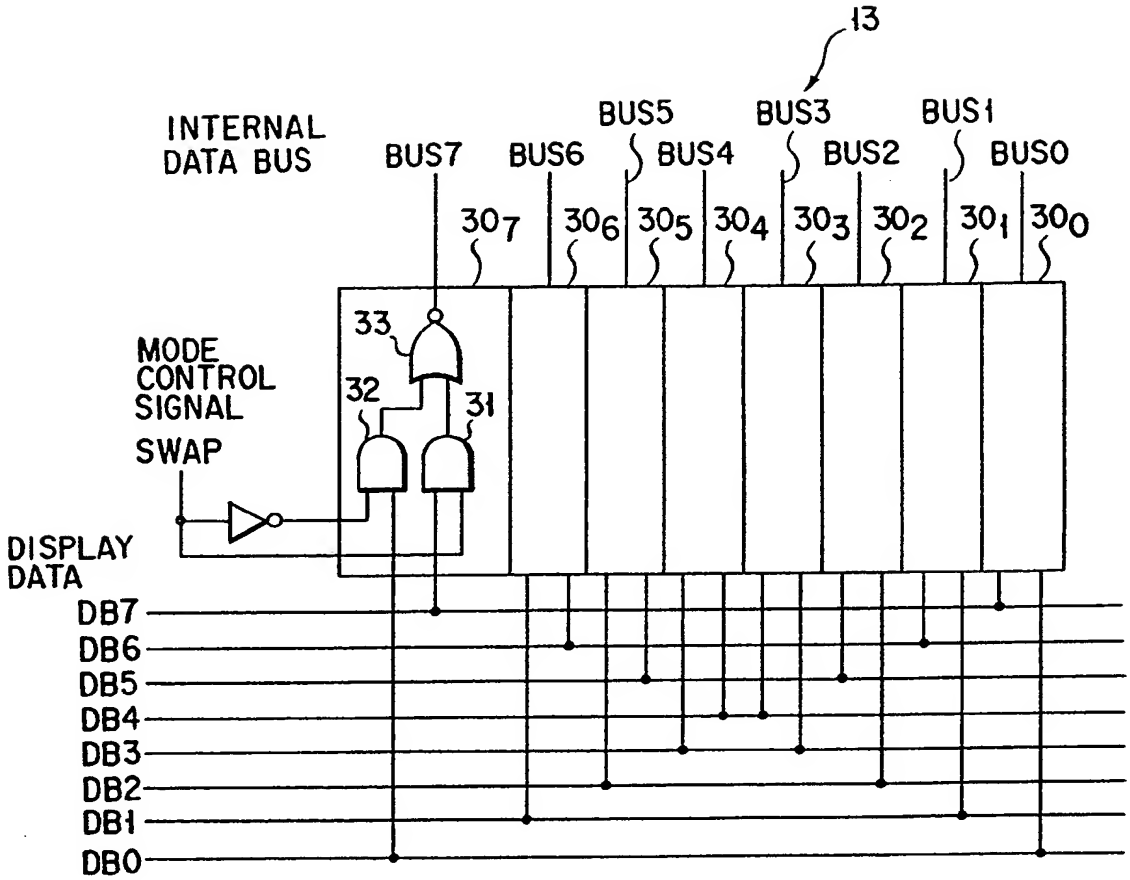


FIG. 5

OUTPUT TERMINAL / MODE	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	-----	S78	S79	S80
NON-INVERTING MODE	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	-----	DB5	DB6	DB7
INVERTING MODE	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-----	DB2	DB1	DB0

FIG. 6



F I G. 7

OUTPUT / SWAP	BUS7	BUS6	BUS5	BUS4	BUS3	BUS2	BUS1	BUS0
SWAP = 0	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
SWAP = 1	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

F I G. 8

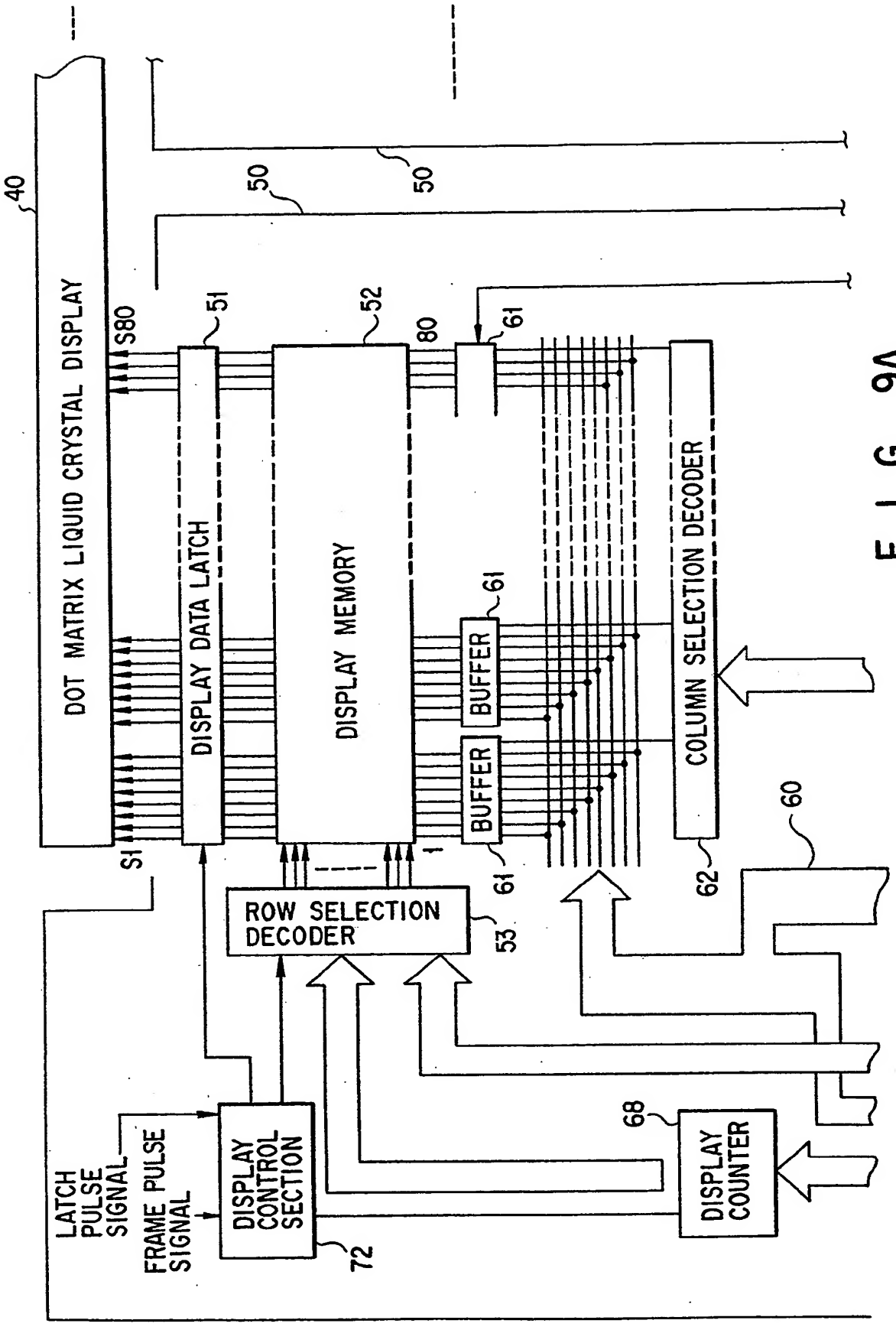


FIG. 9A

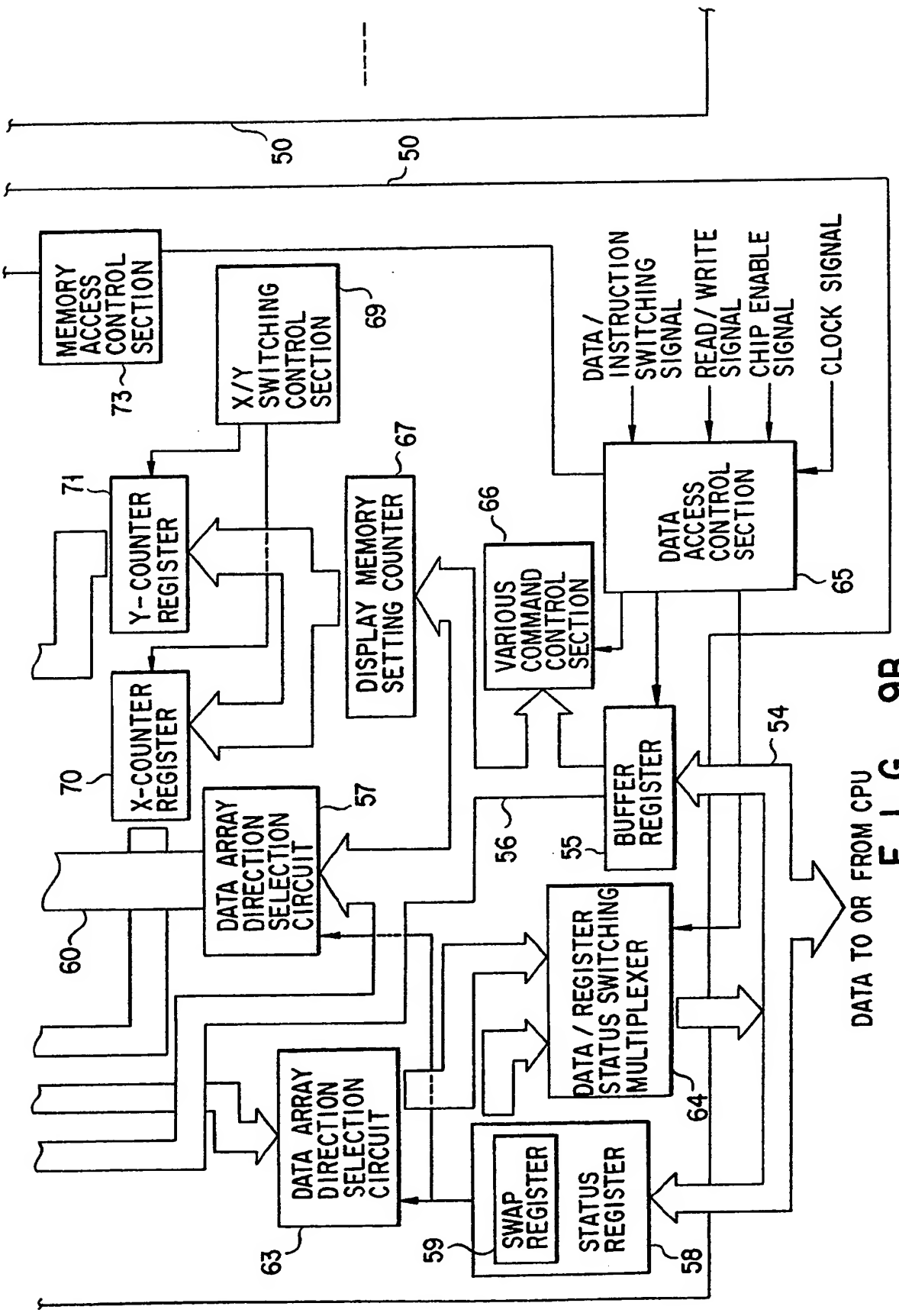


FIG. 9B

"DISPLAY DRIVING/CONTROLLING INTEGRATED CIRCUIT AND DISPLAY SYSTEM"

The present invention relates to a display driving/controlling integrated circuit for supplying display data to a display unit such as a dot matrix display unit for effecting the 2-dimensional image display, and to a display system using the integrated circuit and, more particularly, to a display driving/controlling integrated circuit having a display memory for storing display data.

When a display device such as a dot matrix type liquid crystal display device having a large number of display pixels is driven and controlled, an entire area of the display pixels is divided into a plurality of pixel areas and a display driving/controlling integrated circuit is provided for each divided pixel area.

Fig. 1 is a block diagram showing a display unit and a display driving/controlling integrated circuit. In Fig. 1, X indicates the number of pixels in the column direction of a display unit 90 and Y indicates the number of pixels in the row direction thereof. Further, Xa indicates the number of memory cells in the column direction of a display memory 92 disposed in a display driving/controlling integrated circuit 91 for controlling the display operation of the display unit 90 and Ya indicates the number of memory cells in the row direction thereof. For simplicity, in Fig. 1, only one

display driving/controlling integrated circuit 91 is shown. If the total number of pixels in the display unit 90 is larger than the memory capacity of the display memory in the display driving/controlling integrated circuit 91, for example, if Y > Ya and X > Xa, the display unit 90 cannot be driven by use of only one display driving/controlling integrated circuit 91. Therefore, the entire area of the display pixels of the display unit 90 is divided into a plurality of pixel areas and a plurality of display driving/controlling integrated circuits are used to drive the respective divided pixel areas. In the example of Fig. 1, that area of the display unit 90 which can be driven by one of the display driving/controlling integrated circuits 91 is a partial area A_{XY} indicated by a hatched portion.

As shown in Fig. 2, when the display unit 90 is divided into four areas, four display driving/controlling integrated circuits 91a to 91d are provided to drive the respective four divided areas. The display driving/controlling integrated circuits 91a to 91d are supplied with data DB0 to DB7 from a CPU via a common data bus 93. That is, the four display driving/controlling integrated circuits 91a to 91d are allotted for the four divided areas of the display unit 90.

In order to make the type of integrated circuits uniform and lower the cost thereof, the same type of

integrated circuits with the same arrangement of input terminals for data DB0 to DB7 and output terminals S1 to S80 for driving signals are generally used as the four display driving/controlling integrated circuits 91a to 91d. Since the driving signals output from the output terminals S1 to S80 are supplied to segment lines (not shown) of the display unit 90 and the arrangement of the segment lines of the display unit 90 coincides with the arrangement of the output terminals of the integrated circuit in the two display driving/controlling integrated circuits 91a and 91b which lie below the display unit 90 in Fig. 2, wirings between the display unit and the integrated circuits can be easily made. However, in Fig. 2, since the arrangement of the segment lines of the display unit 90 has an inverted relation with respect to the arrangement of the output terminals of the integrated circuits in the two display driving/controlling integrated circuits 91c and 91d which lie above the display unit 90, a special care must be taken when making wirings between the integrated circuits and the display unit 90.

For example, as shown in Fig. 3, the lower-side display driving/controlling integrated circuits 91a and 91b are mounted on the front surfaces of flexible wiring boards 95 and the wirings formed on the same surface of the flexible wiring boards 95 are connected to the segment lines of the display unit 90 as they are.

However, the upper-side display driving/controlling integrated circuits 91c and 91d are mounted on the rear surfaces of respective flexible wiring boards 95, and in this case, the wirings formed on the rear surfaces of the flexible wiring boards must be re-arranged on the respective front surfaces thereof. At this time, it is required to form through hole connecting portions 95a in the flexible wiring board 95. However, if a necessary flexible wiring board 95 is prepared and the through hole connecting portions 95a are formed therein, the cost will become high. Further, in some cases, it is impossible to form an integrated circuit on the rear surface of the flexible wiring board 95.

The present invention has been made in view of the above drawbacks, and an object of the present invention is to provide a display driving/controlling integrated circuit which can be easily connected with a display unit having a display panel divided into upper and lower sections and a display system using the integrated circuit.

A display driving/controlling integrated circuit of the present invention comprises a display memory for storing data to be supplied to a display unit; a bus line of n-bit configuration for transmitting display data to be stored in the display memory with n bits set as one unit; and a data array direction selection circuit connected to the bus line, for outputting display

data on the bus line to the display memory with the bit array thereof kept in the original bit array status or outputting the display data to the display memory with the bit array thereof inverted with respect to the original bit array.

A display system of the present invention comprises a display unit having a plurality of display pixels which are divided into a plurality of pixel areas; and a plurality of display driving/controlling integrated circuits respectively provided for the plurality of pixel areas of the display unit; each of the plurality of display driving/controlling integrated circuits including a display memory for storing data to be supplied to the display unit, an internal bus line of n-bit configuration for transmitting display data to be stored in the display memory with n bits set as one unit; and a data array direction selection circuit connected to the internal bus line, for outputting display data on the internal bus line to the display memory with the bit array thereof kept in the original bit array status or outputting the display data to the display memory with the bit array thereof inverted with respect to the original bit array status.

In the present invention, the data array direction selection circuit is provided in the preceding stage of the display memory for storing data to be supplied to the display unit and display data on the bus line is

output to the display memory with the bit array thereof kept in the original bit array status or with the bit array thereof inverted with respect to the original bit array by means of the data array direction selection circuit. Therefore, the data array can be changed in the integrated circuit and thus the practical arrangement of the output terminals can be changed in the same type of display driving/controlling integrated circuit.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a display unit and a display driving/controlling integrated circuit;

Fig. 2 is a block diagram showing the construction of a display system using a conventional display driving/controlling integrated circuit;

Fig. 3 is a block diagram showing the construction of a display system using another conventional display driving/controlling integrated circuit;

Fig. 4 is a block diagram showing the construction of a main portion of a display driving/controlling integrated circuit according to the present invention;

Fig. 5 is a block diagram of a display system using the display driving/controlling integrated circuit of Fig. 4;

Fig. 6 is a diagram showing the bit array status of

data output from the display driving/controlling integrated circuit of Fig. 4;

Fig. 7 is a circuit diagram showing the detail construction of a data array direction selection circuit in the display driving/controlling integrated circuit of Fig. 4;

Fig. 8 is a diagram showing the bit array status of data output from the data array direction selection circuit of Fig. 7; and

Figs. 9A and 9B are block diagrams showing the detail construction of the display system of Fig. 5.

There will now be described an embodiment of a display driving/controlling integrated circuit and an embodiment of a display system according to this invention with reference to the accompanying drawings.

Fig. 4 is a block diagram showing the construction of the main portion of a display driving/controlling integrated circuit 21 according to the present invention. As shown in Fig. 4, a display memory 11 formed of a RAM containing display image data is provided in the display driving/controlling integrated circuit 21. For example, memory cells (not shown) are arranged in a matrix form with 80 rows and 64 columns in the display memory 11. Signals output from 80 output signal terminals S1 to S80 of the display memory 11 are supplied to segment lines of one of equally divided areas of a display unit (not shown). For example, 10 buffers 12

each having an 8-bit input/output capacity are provided on the input side of the display memory 11. The 10 buffers 12 are connected to internal data buses BUS0 to BUS7 of 8-bit configuration, for example.

The internal data buses BUS0 to BUS7 are supplied with outputs of a data array direction selection circuit 13. The data array direction selection circuit 13 is supplied with display data items DB0 to DB7 of plural bits, for example, 8 bits and outputs the display data items DB0 to DB7 to the internal data buses BUS0 to BUS7 after controlling the array status of the display data items DB0 to DB7 according to the logic level of a mode control signal SWAP supplied from a mode control signal supplying means 15. For example, the data array direction selection circuit 13 outputs the input data items DB0 to DB7 to the internal buses BUS0 to BUS7 as they are with the bit array status thereof kept unchanged when the mode control signal SWAP is set at the "1" level indicating the non-inverting mode, and outputs the input data items DB0 to DB7 to the internal buses BUS0 to BUS7 after inverting the bit array status thereof when the mode control signal SWAP is set at the "0" level indicating the inverting mode. That is, whether the array direction of data bits is kept unchanged or inverted is determined by the mode control signal SWAP when display data is written into the display memory 11 from the buffer 12. An address signal for the display

memory 11 is input to a selection decoder 14 to specify a display area of the display memory 11. The 10 buffers 12 are supplied with outputs of the selection decoder 14. Each of the buffers 12 permits a storage area for the memory to be selected according to an address signal output of the selection decoder 14 and selectively takes in 8-bit data transferred via the internal data buses BUS0 to BUS7. The 8-bit data stored in each of the buffers 12 is output and stored into a corresponding display area of the display memory 11 at a preset timing.

Fig. 5 is a block diagram showing the schematic construction of a display system using the display driving/controlling integrated circuit 21 of Fig. 4. In this display system, each of divided areas of the entire display pixel area of the display unit is driven by means of a corresponding one of display driving/controlling integrated circuits 21. For example, in order to drive a display unit 20 in which the display panel is divided into upper and lower sections and display pixels are equally divided into four areas as in the display system shown in Fig. 5, four display driving/controlling integrated circuits having the same construction as the display driving/controlling integrated circuit of Fig. 4 are used. In Fig. 5, the four display driving/controlling integrated circuits are denoted by reference numerals 21a to 21d.

In the display driving/controlling integrated circuit 21 with the above construction, the data array direction selection circuit 13 outputs input data items DB0 to DB7 to the internal buses BUS0 to BUS7 as they are with the array status thereof kept unchanged when the mode control signal SWAP is set at the "1" level indicating the non-inverting mode. That is, the least significant bit data DB0 is output to the internal data bus BUS0 of the least significant bit position and the most significant bit data DB7 is output to the internal data bus BUS7 of the most significant bit position. Then, 8-bit data which is first output to the internal buses BUS0 to BUS7 is stored into one of the buffers 12 which is disposed on the leftmost position according to the output of the selection decoder 14 and then stored into a preset storage area of the display memory 11. Likewise, each time 8-bit data is supplied, the data array direction selection circuit 13 outputs input data items DB0 to DB7 to the internal buses BUS0 to BUS7 with the array status thereof kept unchanged and the 8-bit data transferred via the internal data buses BUS0 to BUS7 is sequentially stored into the remaining 9 buffers 12 which are disposed on the right-hand side of the buffer into which the 8-bit data has been first stored. Thus, after 8-bit data is supplied to the data array direction selection circuit 13 ten times, data will be stored into all of the memory cells or 80 memory cells

of one column of the display memory 11. After data is thus stored into all of the rows of the display memory 11, previously stored data is read out to drive the display unit 20. In the readout operation, the relation indicating the non-inverting mode as shown in Fig. 6 can be set up between signals output from the 80 output terminals S1 to S80 and 8-bit input data items DB0 to DB7. That is, the array status of the output signals of the output terminals S1 to S80 is set to correspond to the array status of the input data items obtained by serially arranging groups of 8-bit input data items DB0 to DB7 without changing the array direction of the input data items DB0 to DB7 supplied to the data array direction selection circuit 13.

On the other hand, in the display driving/controlling integrated circuit 21, when the mode control signal SWAP is set at the "0" level indicating the inverting mode, the data array direction selection circuit 13 outputs the input data items DB0 to DB7 to the internal buses BUS0 to BUS7 after inverting the array status thereof. That is, the least significant bit data DB0 is output to the internal data bus BUS7 of the most significant bit position and the most significant bit data DB7 is output to the internal data bus BUS0 of the least significant bit position. Then, when data is read out after data is stored into all of the rows of the display memory 11, the relation indicating the inverting

mode as shown in Fig. 6 is set up between signals output from the 80 output terminals S1 to S80 of the display memory 11 and 8-bit input data items DB0 to DB7. That is, the array status of the output signals of the output terminals S1 to S80 is set to correspond to the array status of the input data items obtained by serially arranging groups of 8-bit input data items DB0 to DB7 in a reverse order with the array direction of the input data items DB0 to DB7 inverted with respect to the initial array direction of the 8-bit input data items DB0 to DB7 supplied to the data array direction selection circuit 13. Therefore, in the display driving/controlling integrated circuit 21 in which the mode control signal SWAP is set at the "0" level, the bit array of data output from the output terminals S1 to S80 is inverted with respect to that in the display driving/controlling integrated circuit 21 in which the mode control signal SWAP is set at the "1" level.

In order to drive the display unit 20 of Fig. 5, four display driving/controlling integrated circuits which have the same construction as the display driving/controlling integrated circuit 21 of Fig. 4 are used, the mode control signal SWAP is set at the "1" level to set the non-inverting mode in two display driving/controlling integrated circuits 21a and 21b which are arranged on the lower side of the display unit 20, and the mode control signal SWAP is set at the "0"

level to set the inverting mode in two display driving/controlling integrated circuits 21c and 21d which are arranged on the upper side of the display unit 20. As a result, the array of signals output from the output terminals S80 to S1 of the two display driving/controlling integrated circuits 21c and 21d which are set in the inverting mode becomes equal to the array of signals output from the output terminals S1 to S80 of the two display driving/controlling integrated circuits 21a and 21b which are set in the non-inverting mode. Therefore, as shown in Fig. 5, the upper-side display driving/controlling integrated circuits 21c and 21d and the lower-side display driving/controlling integrated circuits 21a and 21b can be arranged along the upper and lower columns of the display unit 20. As a result, the output terminals S1 to S80 of the two display driving/controlling integrated circuits 21c and 21d disposed on the upper side of the display unit 20 can be directly connected to segment lines of the display unit 20 like the two display driving/controlling integrated circuits 21a and 21b disposed on the lower-side of the display unit 20. Thus, unlike the conventional case, in the present invention, it is not necessary to form through hole connecting portions in the flexible wiring board and the connection between the display driving/controlling integrated circuits 21a to 21d and the display unit 20 can be easily made.

Fig. 7 is a circuit diagram showing the detail construction of the data array direction selection circuit 13 according to the embodiment of Fig. 4. The data array direction selection circuit 13 includes 8 data selection circuits 30_0 to 30_7. As typically shown by the data selection circuit 30_7, each of the data selection circuits includes two 2-input AND gates 31 and 32, and a NOR gate 33 supplied with outputs of the AND gates 31 and 32. An inverted signal of the mode control signal SWAP is commonly supplied to the first input terminals of the AND gates 31 of all of the data selection circuits 30_0 to 30_7 and the mode control signal SWAP is commonly supplied to the first input terminals of the AND gates 32. In the data selection circuit 30_7, the second input terminal of the AND gate 31 is supplied with the input data DB7 and the second input terminal of the AND gate 32 is supplied with the input data DB0. In the data selection circuit 30_6, the second input terminal of the AND gate 31 is supplied with the input data DB6 and the second input terminal of the AND gate 32 is supplied with the input data DB1. In the data selection circuit 30_5, the second input terminal of the AND gate 31 is supplied with the input data DB5 and the second input terminal of the AND gate 32 is supplied with the input data DB2. In the data selection circuit 30_4, the second input terminal of the AND gate 31 is supplied with the input data DB4 and the second input terminal of

the AND gate 32 is supplied with the input data DB3. In the data selection circuit 30_3, the second input terminal of the AND gate 31 is supplied with the input data DB3 and the second input terminal of the AND gate 32 is supplied with the input data DB4. In the data selection circuit 30_2, the second input terminal of the AND gate 31 is supplied with the input data DB2 and the second input terminal of the AND gate 32 is supplied with the input data DB5. In the data selection circuit 30_1, the second input terminal of the AND gate 31 is supplied with the input data DB1 and the second input terminal of the AND gate 32 is supplied with the input data DB6. In the data selection circuit 30_0, the second input terminal of the AND gate 31 is supplied with the input data DB0 and the second input terminal of the AND gate 32 is supplied with the input data DB7. Outputs of the NOR gates 33 of the data selection circuits 30_0 to 30_7 are respectively supplied to the internal data buses BUS0 to BUS7.

When the mode control signal SWAP is set at the "1" level to set the non-inverting mode in the data array direction selection circuit 13, the AND gate 31 of each of the data selection circuits is selected. Therefore, the input data items DB0 to DB7 are output to the internal data buses BUS0 to BUS7 with the array status thereof kept unchanged. However, the logic levels of the data items output to the internal data buses BUS0 to

BUS7 are inverted with respect to those of the original input data items DB0 to DB7. When the mode control signal SWAP is set at the "0" level to set the inverting mode, the AND gate 32 of each of the data selection circuits is selected. Therefore, the input data items DB0 to DB7 are output to the internal data buses BUS0 to BUS7 with the array thereof inverted with respect to the initial data array.

Fig. 8 shows the array status of data items output to the internal data buses BUS0 to BUS7 in the non-inverting and inverting modes.

Figs. 9A and 9B are block diagrams showing the detail constructions of the embodiment of the display system. In this example, a dot matrix liquid crystal display unit 40 having XP pixels in the column direction and YP pixels in the row direction is used as the display unit. The display unit 40 is driven by means of a plurality of display driving/controlling integrated circuits as described before, but for brief explanation, only one display driving/controlling integrated circuit 50 is shown in detail in Fig. 9A. In Fig. 9A, 51 denotes a display data latch for supplying segment signals to the display unit 40. The display data latch 51 is supplied with display data read out from a display memory 52 corresponding to the display memory 11 of Fig. 4. The display memory 52 has memory cells (not shown) arranged in one-to-one correspondence to the

pixels of the display unit 40. Numbers of bit 1 to bit 80 are attached to input lines of the display memory 52. Therefore, 80 output terminals of S1 to S80 are used for segment signals of the display driving/controlling integrated circuit 50. When the number of memory cells in the column direction of the display memory 52 is XM and the number of memory cells in the row direction is YM, and if XM < YP and YM < YP, then a plurality of display driving/controlling integrated circuits 50 are necessary to drive the display unit 40. Display data previously stored in the display memory 52 is selected in the unit of row in response to an output of the row selection decoder 53 and the readout data is supplied to the display data latch 51 as segment driving signals.

In Fig. 9B, 54 denotes an external data bus for transferring data output from an external CPU (not shown). Display data on the external data bus 54 is supplied to a buffer register 55 and then input to a data array direction selection circuit 57 corresponding to the data array direction selection circuit 13 via a first internal data bus 56. Then, the data array direction is selected according to the mode control signal SWAP output from a SWAP register 59 which is one of the registers in a status register 58. An output of the data array direction selection circuit 57 is commonly supplied to 10 buffers 61 corresponding to the buffers 12 of Fig. 4 via a second internal data bus 60

corresponding to the internal data buses BUS0 to BUS7 of Fig. 4. Then, 8-bit display data transferred on the second internal data bus 60 is stored into one of the 10 buffers 61 according to an output of a column selection decoder 62 corresponding to the selection decoder 14 of Fig. 4. Further, data is stored into 8-bit memory cells of the display memory 52 which are selected by outputs of the column selection decoder 62 and the row selection decoder 53.

It is also possible to read out data from the display memory 52 and supply the readout data to the 10 buffers 61, and 8-bit memory cells of the display memory 52 from which data is read out are selected by outputs of the column selection decoder 62 and the row selection decoder 53. The readout data is supplied to the external CPU via a readout data array direction selection circuit 63, a data/register switching multiplexer 64 and the external data bus 54.

The multiplexer 64 is supplied with outputs of the data array direction selection circuit 63 and the status register 58. The operation of the data/register status switching multiplexer 64 is controlled by a data access control section 65. The data access control section 65 is supplied with a data/instruction switching signal, read/write signal, chip enable signal and clock signal and determines whether data input to the external data bus 54 from the external CPU is display data or other

data such as an instruction or various commands. When the data is an instruction, data on the first internal data bus 56 is input to a various command control section 66 under the control of the data access control section 65 without being stored into the buffer 61. Further, data on the first internal data bus 56 for controlling the operations of the row selection decoder 53 and column selection decoder 62 is input to a display memory setting counter 67 or display counter 68 under the control of the data access control section 65. An output of the display memory setting counter 67 is selectively input to an X-counter register 70 or Y-counter register 71 according to an output of an X/Y switching control section 69. An output of the X-counter register 70 is input to the row selection decoder 53 and an output of the Y-counter register 71 is input to the column selection decoder 62.

The operation of the row selection decoder 53 for selecting a row of the display memory 52 at the data readout/write-in time is controlled by outputs of the X-counter register 70 and display counter 68 and an output of the display control section 72. Further, the display control section 72 is supplied with a latch pulse signal for controlling the latching operation of the display data latch 51 and a frame signal for controlling the display operation. An output of the data access control section 65 is supplied to a memory access control

section 73 and the data readout/write-in operation of the buffers 61 is selected under the control of the memory access control section 73.

In the integrated circuit of this embodiment, data in the display memory 52 and the status in the status register 58 can be read out. For example, data in an area of the display memory 52 specified by outputs of the row selection decoder 53 and the column selection decoder 62 is output to the second internal data bus 60 via one of the buffers 61. Data on the second internal data bus 60 is input to the readout data array direction selection circuit 63. The data array direction selection circuit 63 is also supplied with the mode control signal SWAP of the SWAP register 59 of the status register 58. Therefore, 8-bit data read out from the display memory 52 is set into the bit array status which is the same as or inverted with respect to the original status set at the readout time by means of the data array direction selection circuit 63 and the output thereof is output to the external data bus 54 via the data/register status switching multiplexer 64.

That is, even in the inverting mode in which the mode control signal SWAP of the SWAP register 59 is set at the "0" level, when data is read out from the display memory 52 and output to the exterior, the bit array of the data is set to the same bit array status set when data is input from the exterior.

The X-counter register 70 and Y-counter register 71 have the increment/decrement functions for sequentially specifying display memory areas when display data is written into the display memory 52. The increment function is to sequentially increase the content thereof one by one from the initial value and the decrement function is to decrease the content thereof one by one. The increment/decrement functions of the X-counter register 70 and Y-counter register 71 can be set by inputting an instruction from the exterior in the same manner as in the case of the SWAP register 59. The increment/decrement operation is automatically effected after the operation of writing data into the areas of the display memory 52 is completed.

Data with the inverted bit array direction with respect to the bit array direction of whole 8-bit data inputted into the integrated circuit can be readily used as display data by use of a combination of the bit array control based on the content of the SWAP register 59 used for selecting the bit array status of 8-bit data and the increment/decrement selection function of the counter register 71. At this time, the address setting for writing data into the display memory 52 is automatically effected in the X-counter register 70 and Y-counter register 71. Therefore, when data is written into the display memory 52, it is not necessary for the CPU to calculate the address. For example, the bit

array direction of output data supplied to the display unit 40 set when the Y-counter register 71 is selected by the X/Y switching control section 69, the content of the SWAP register 59 indicates the inverting mode and the decrement function of the register 71 is selected is opposite to the bit array direction of the output data set when the content of the SWAP register 59 indicates the non-inverting mode and the increment function is selected in the register 71.

Claims:

1. A display driving/controlling integrated circuit comprising:

a display memory for storing and outputting data to be supplied to a display unit;

a bus line of n-bit configuration for transmitting display data to be stored in said display memory with n bits set as one unit;

mode control signal supplying means for supplying a mode control signal for changing the bit array status of the display data; and

a data array direction selection circuit connected to said bus line, for outputting display data on said bus line to said display memory with the bit array thereof set in one of the original bit array status and the bit array status inverted with respect to the original bit array status.

2. A display driving/controlling integrated circuit according to claim 1, further comprising a plurality of buffers connected to said display memory, for permitting a storage area of said display memory designated by a specified address to be selected.

3. A display driving/controlling integrated circuit according to claim 1, wherein said data array direction selection circuit includes n data selection circuits each of which includes first and second AND gates and an OR gate having input terminals connected to

the output terminals of said first and second AND gates; a first input terminal of each of said first AND gates of said n data selection circuits being supplied with a selection signal, a second input terminal of each of said first AND gates being supplied with a corresponding one of bits of the n-bit display data arranged in an order from the most significant bit to the least significant bit, a first input terminal of each of said second AND gates of said n data selection circuits being supplied with an inverted signal of the selection signal, and a second input terminal of each of said second AND gates being supplied with a corresponding one of bits of the n-bit display data arranged in an order from the least significant bit to the most significant bit.

4. A display system comprising:

a display unit having a plurality of display pixels which are arranged in row and column directions in a matrix form and which are divided into upper and lower display panels; and

a plurality of display driving/controlling integrated circuits for driving and controlling said display pixels, those of said display driving/controlling integrated circuits provided on the lower side of said lower display panel outputting display data with a preset bit array, and those of said display driving/controlling integrated circuits provided on the

upper side of said upper display panel outputting display data with a bit array inverted with respect to the preset bit array.

5. A display system according to claim 4, wherein each of said upper and lower display panels is divided into a plurality of areas and said plurality of display driving/controlling integrated circuits are respectively provided for said plurality of areas.

6. A display system according to claim 4, wherein each of said plurality of display driving/controlling integrated circuits includes:

a display memory for storing data to be supplied to said display unit;

an internal bus line of n-bit configuration for transmitting display data to be stored in said display memory with n bits set as one unit;

mode control signal supplying means for supplying a mode control signal for changing the bit array status of the display data; and

a data array direction selection circuit connected to said internal bus line, for outputting display data on said bus line to said display memory with the bit array thereof set in one of the original bit array status and the bit array status inverted with respect to the original bit array status.

7. A display system according to claim 4, wherein said data array direction selection circuit includes n

data selection circuits each of which includes first and second AND gates and an OR gate having input terminals connected to the output terminals of said first and second AND gates; a first input terminal of each of said first AND gates of said n data selection circuits being supplied with selection information, a second input terminal of each of said first AND gates being supplied with a corresponding one of bits of the n-bit display data arranged in an order from the most significant bit to the least significant bit, a first input terminal of each of said second AND gates of said n data selection circuits being supplied with information having a complementary relation with respect to the selection information, and a second input terminal of each of said second AND gates being supplied with a corresponding one of bits of the n-bit display data arranged in an order from the least significant bit to the most significant bit.

8. A display system according to claim 7, wherein said plurality of display driving/controlling integrated circuits include storing means for storing the selection information.

9. A display driving/controlling integrated circuit, substantially as hereinbefore described with reference to Fig. 4 of the accompanying drawings.

10. A display system, substantially as hereinbefore described with reference to Fig. 9 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number: 9206597.8

Relevant Technical fields

(i) UK Cl (Edition K) G5C (CHB)

(ii) Int Cl (Edition 5) G09G

Search Examiner: G M PITCHMAN

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASE: WPI

Date of Search: 7 AUGUST 1992

Documents considered relevant following a search in respect of claims 1 TO 10

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 2106689 A (SHARP) See Figure 1	1
A	EP 0216188 A2 (CANON) See abstract	4
A	EP 0055676 A2 (SANGAMO WESTON) See abstract	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Published 1992 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Sales Branch, Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd, St Mary Cray, Kent.

)OCID: <GB___2255668A__I_>

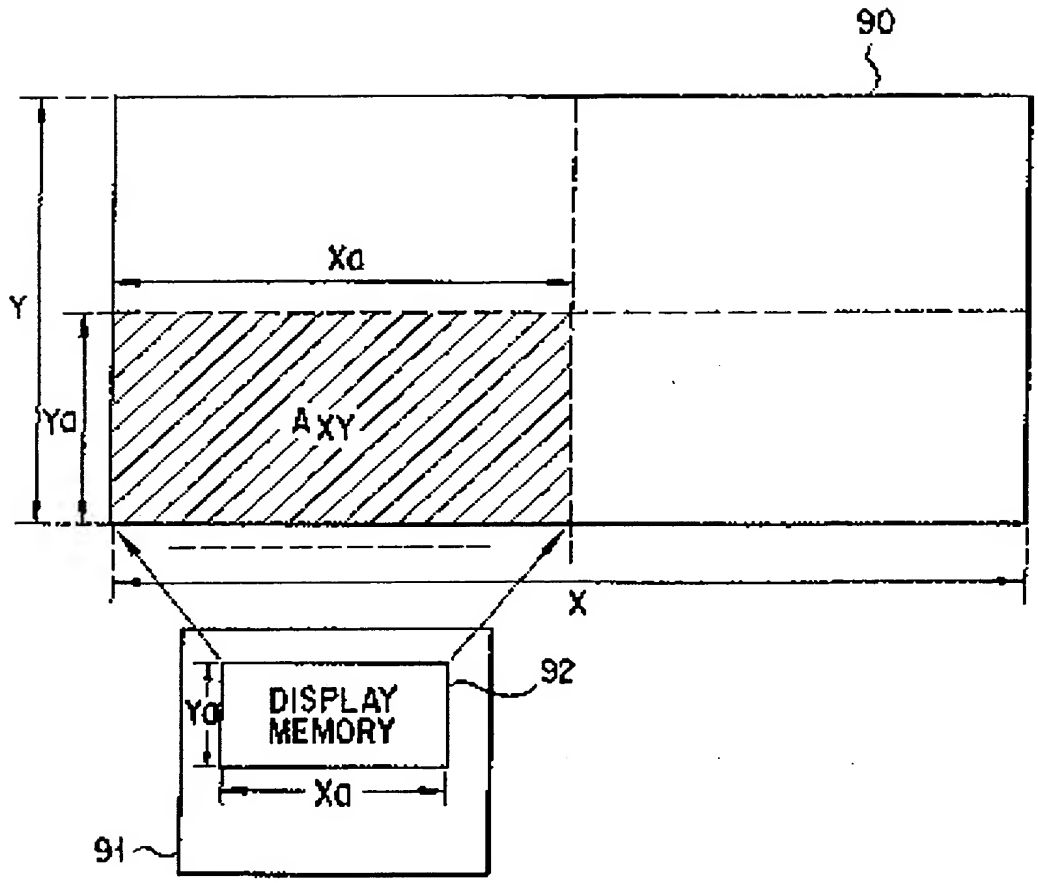


FIG. 1

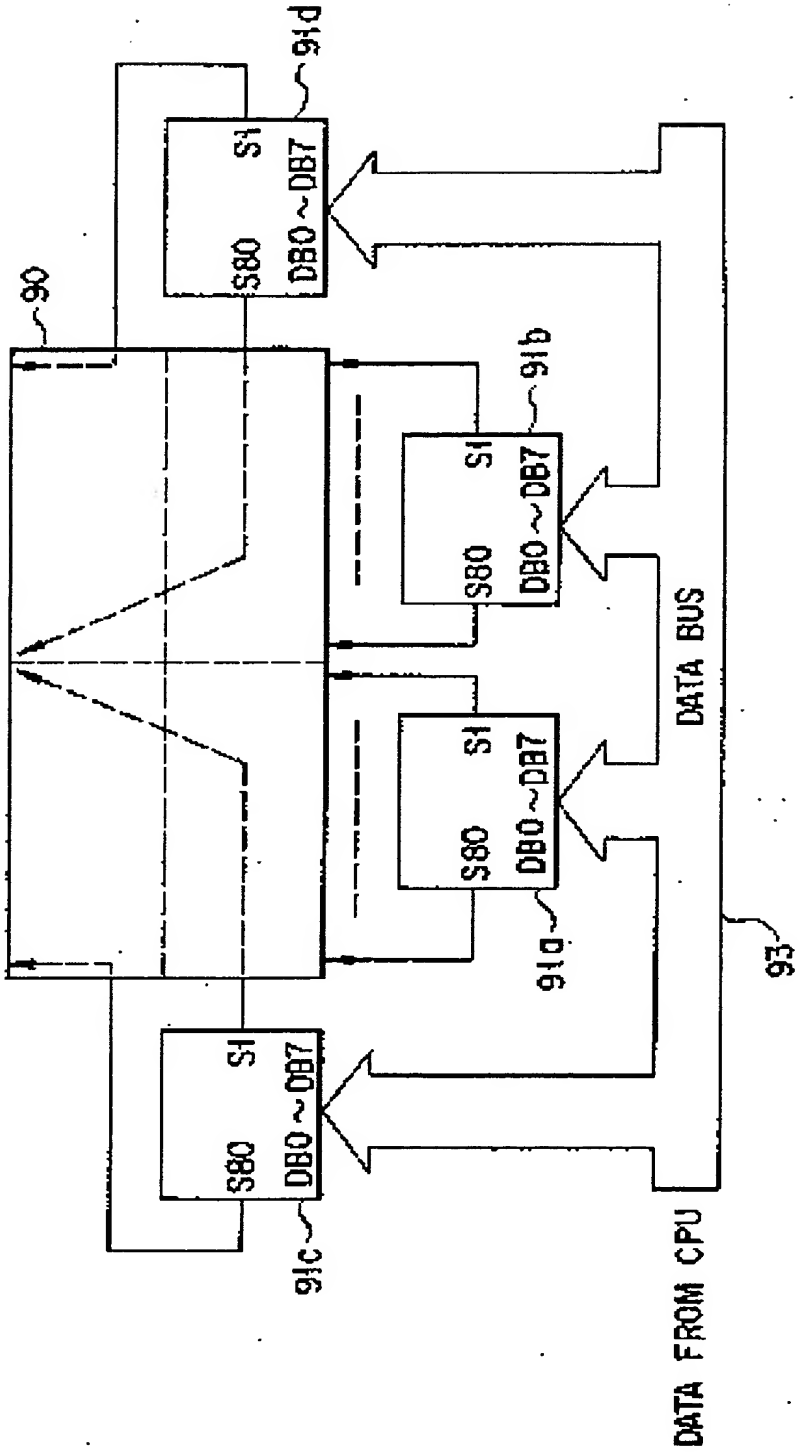


FIG. 2

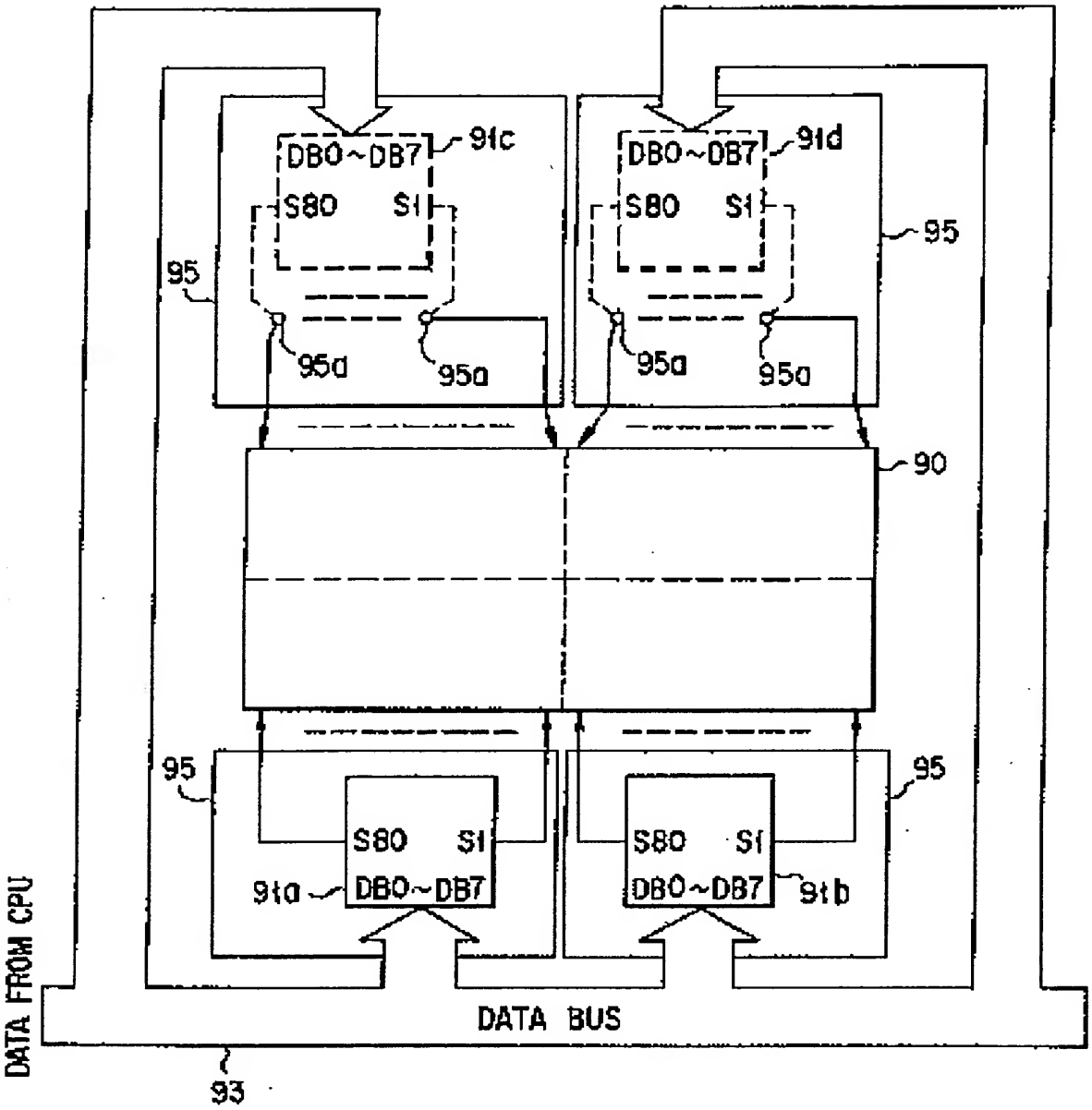


FIG. 3

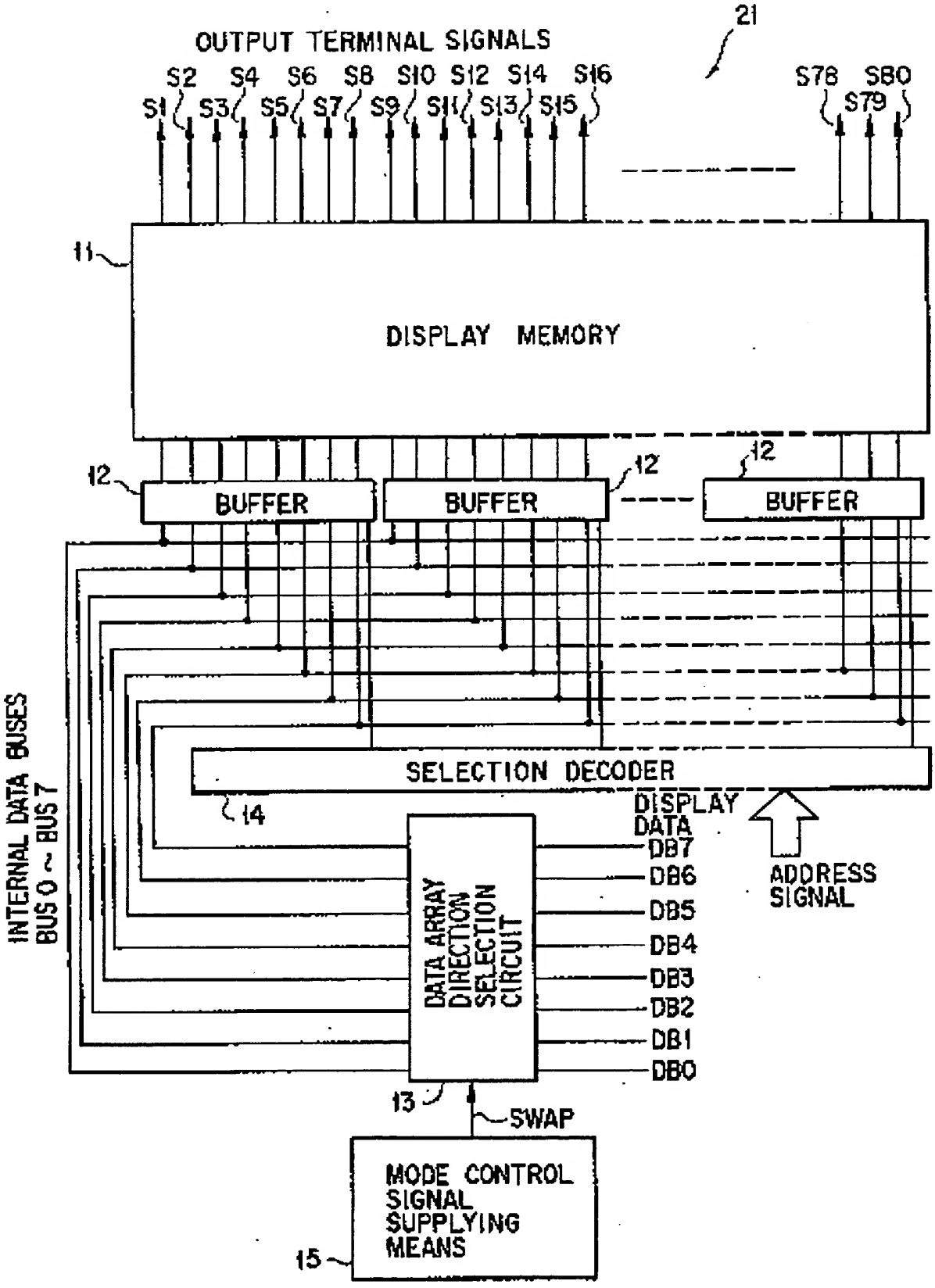


FIG. 4

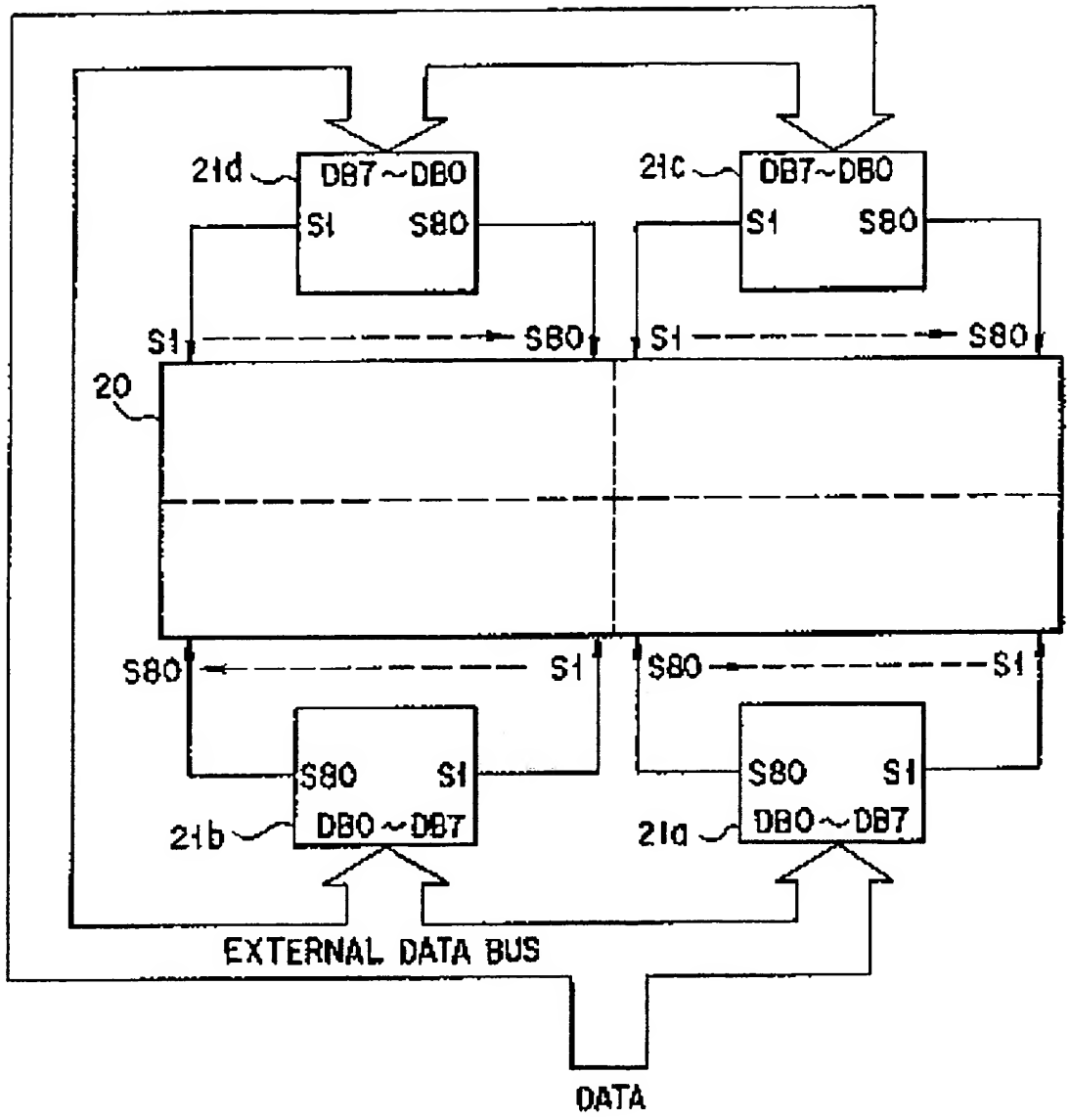
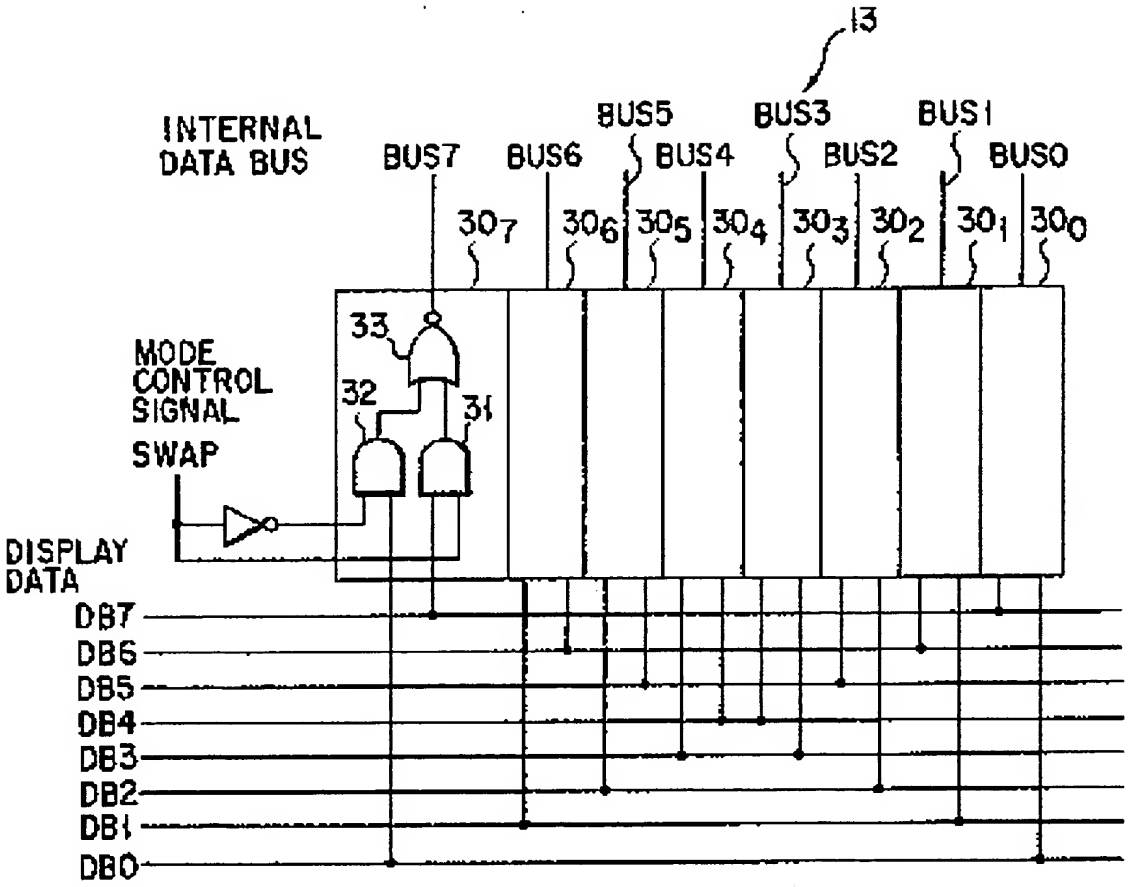


FIG. 5

OUTPUT TERMINAL / MODE	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	-----	S78	S79	S80
NON-INVERTING MODE	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	-----	DB5	DB6	DB7
INVERTING MODE	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-----	DB2	DB1	DB0

F I G. 6



F I G. 7

SWAP \ OUTPUT	BUS7	BUS6	BUS5	BUS4	BUS3	BUS2	BUS1	BUS0
SWAP = 0	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
SWAP = 1	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

F I G. 8

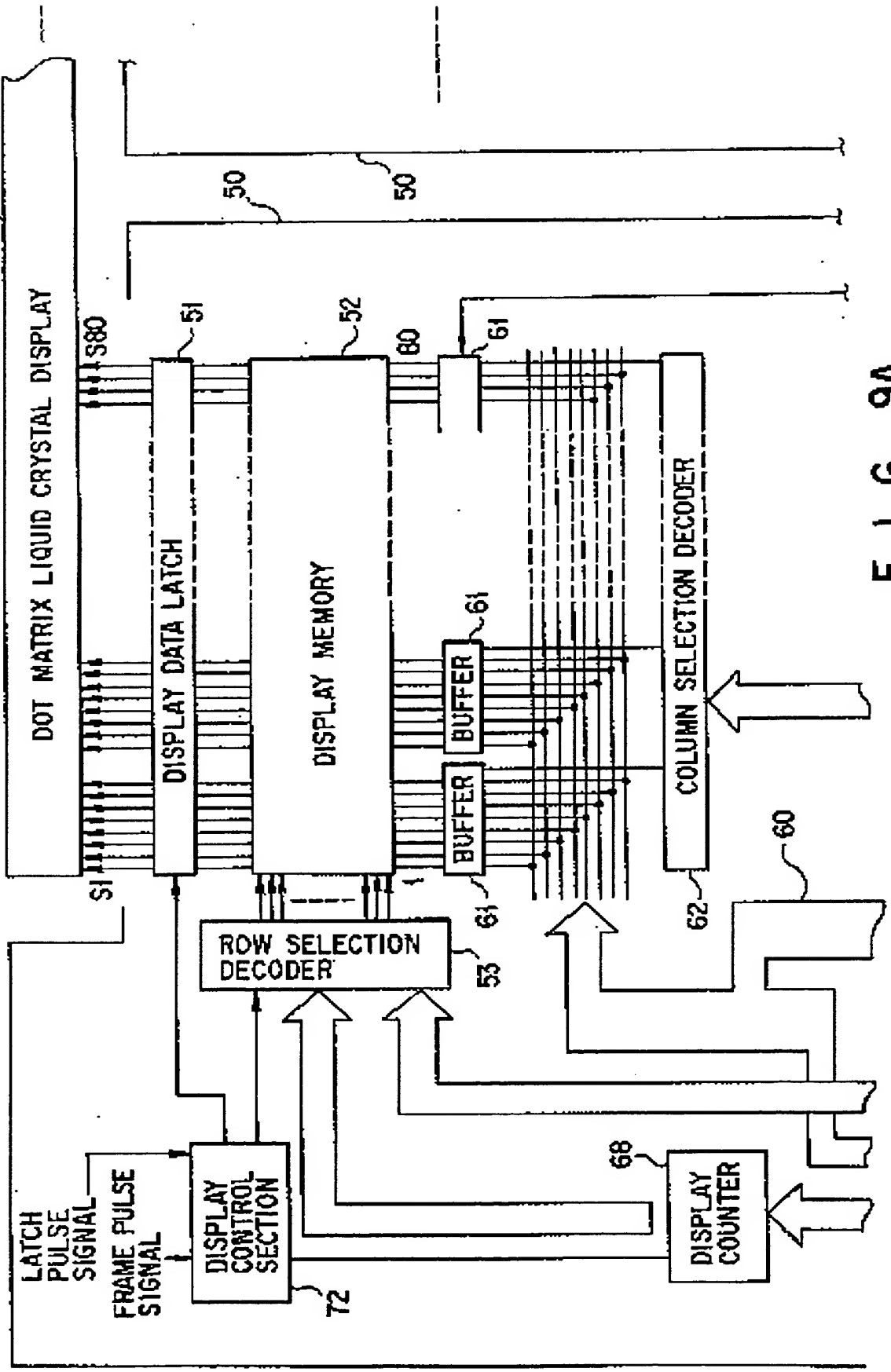


FIG. 9A

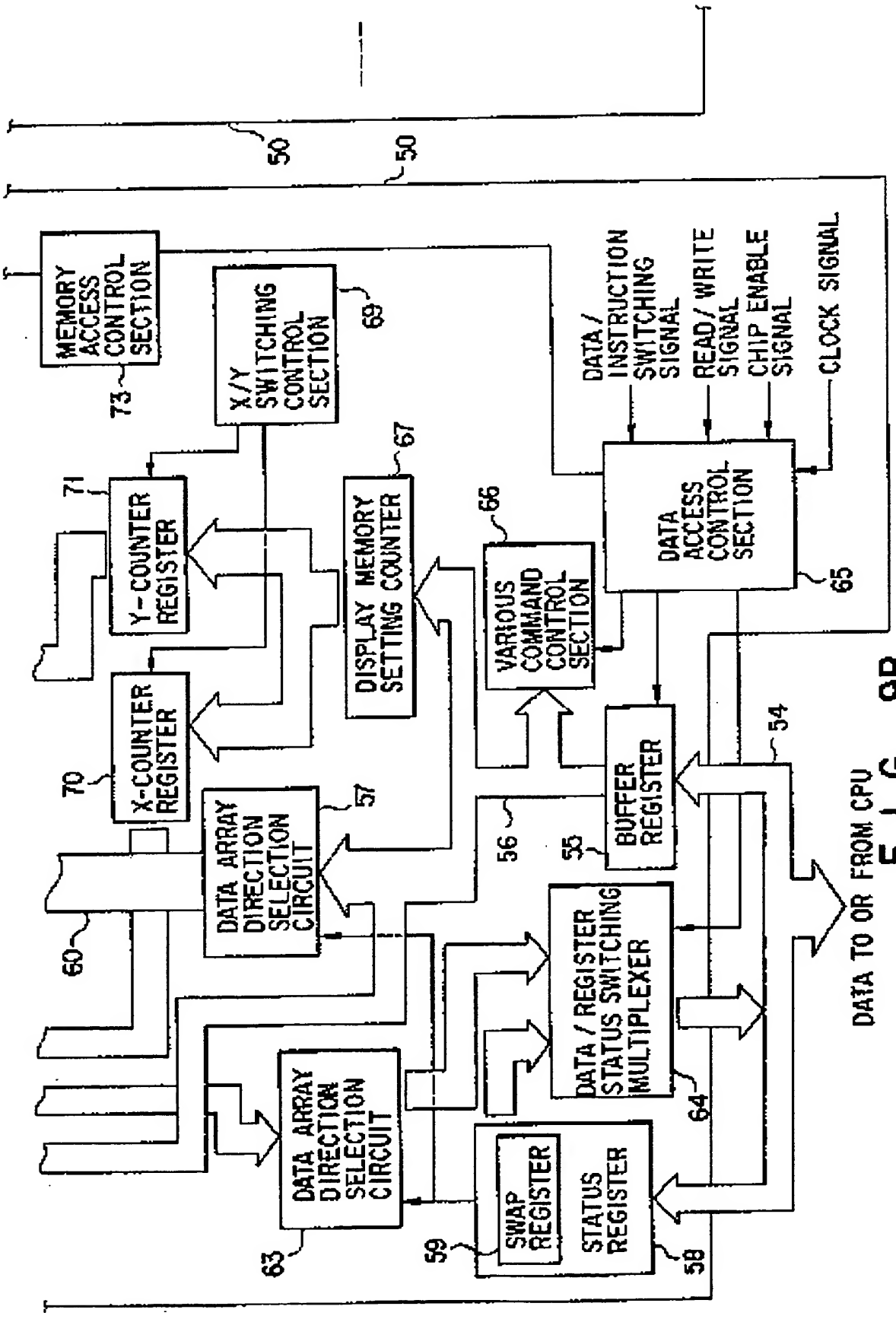


FIG. 9B

THIS PAGE BLANK (USPTO